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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/666,257	09/21/2000	Adrian Yap	PD-200057	8880
20991	7590	12/17/2004	EXAMINER	
THE DIRECTV GROUP INC			BOCCIO, VINCENT F	
PATENT DOCKET ADMINISTRATION RE/R11/A109			ART UNIT	PAPER NUMBER
P O BOX 956				2616
EL SEGUNDO, CA 90245-0956				

DATE MAILED: 12/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	09/666,257	YAP ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Vincent F. Boccio	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

**A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.**

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) Responsive to communication(s) filed on 9/21/00 ✓  
 2a) This action is FINAL.                    2b) This action is non-final.  
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) Claim(s) 1-39 is/are pending in the application.  
 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
 5) Claim(s) \_\_\_\_\_ is/are allowed.  
 6) Claim(s) 1-12, 15, 18-23, 28, 32, 33, 37-39 is/are rejected.  
 7) Claim(s) 13, 14, 16, 17, 24-27, 29-31 and 34-36 is/are objected to.  
 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) The specification is objected to by the Examiner.  
 10) The drawing(s) filed on \_\_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All    b) Some \* c) None of:  
 1. Certified copies of the priority documents have been received.  
 2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
|  | 6) <input type="checkbox"/> Other: _____                                    |

**DETAILED ACTION**

The Group and/or Art Unit location of your application in the PTO has changed. To aid in correlating any papers for this application, all further correspondence regarding this application should be directed to Group Art Unit 2616.

**Claim Rejections - 35 USC § 103**

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 1-12, 15, 18-23, 28, 32-33 and 37-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chauvel et al. (US 6,369,855) in view of Muto (US 5,799,129).

Regarding claim 1, Chauvel discloses and meets the limitations associated with an apparatus for performing reverse playback of digitally recorded coded audiovisual data comprising:

- a memory operatively connected to a bus for storing the digitally recorded coded audiovisual data (Fig. 1 b, traffic controller with memory, "SRAM, DRAM, SDRAM", reference Fig. 12, "210 to 310 to 1394 thru arm bus"

Art Unit: 2616

col. 17, "The packet coming out of TPP 210 can go either to the 1394 interface 290 or to the RAM 240 thru the traffic controller TC or to both at the same time. This allows for the circuit 200 to decode one program while recording ...", therefore, from the traffic controller memory to decoder Fig. 1 b and to arm bus to 1394 for recording and decoding the same simultaneously;

- a graphics accelerator operatively connected to the bus and to a decoder ("BitBIT H/W Accelerator/OSD", outputting a digital video stream etc.....);
- a decoder (Fig. 1 B, "decoder 250", for decoding the coded from the memory (thru traffic controller memory to 250, Fig. 12, Fig. 1B and col. 17 & col.19, lines 14-20 etc..... and to 1394 memory device);
- wherein the output of the graphics controller provides video frames in the reverse order as claimed (col. 5, play mode - reverse).

Chauvel provides for reverse playback, but, fails to disclose wherein the graphics accelerator temporally reversing the decoded order of the audiovisual data of its memory and outputting in reverse the decoded data as a displayed reverse playback.

Muto teaches with respect to Fig. 1, a process as shown in Figs. 3 A-c etc., wherein the output of the MPEG decoder is provided with a plurality of memory areas, as shown in Fig. 3 C, could be 4 areas or more (other embodiments), wherein the memory receives the data according to Fig. 3 B, stores in areas, as shown in Fig. 3 C, holding a plurality of frames, wherein upon selecting reverse playback mode (col. 4, lines 5-13, "writing the decoded data in the frame buffer means, then reading out the data from the frame buffer means in the reverse order of the original pictures and displaying the read out, also reference col. 7, lines 3 to col. 8, line 23, "The decoded stored in the buffer 2-3 supplied to the display in the reverse order of the original and are displayed"), having the advantage of performing special playback without the necessity of raising a coded data

Art Unit: 2616

transfer rate to a decoder or increase the storage capacity of a frame memory either (col. 3, lines 57-), as taught by Muto.

The examiner further takes official notice that video accelerators are known to perform various tasks offloaded from the main CPU or processing element, wherein video accelerators are known for handling video decoding, such as decompression, known to also be advantageous in hardware form or hybrid forms, part software and part hardware, as is well known to those skilled in the art.

Therefore, it would have been obvious to one skilled in the art at the time of the invention to modify Chauvel by incorporating an video accelerator with memory to offload the decoding processing, storing in the memory decoded pictures received in the forward direction, upon a reverse command for reverse reproduction operation, to reverse the order from the memory, to initiate and achieve reverse operation utilizing more than I frames or using P and well as B frames, realizing natural reproduced pictures on the display without raising the rate or capacity of a frame memory, as taught by Muto.

Regarding claims 2-3, Muto further provides for a recording and reproduction device (recording thru 1394), and further meets the limitations of wherein the recording device meets the limitation of mass storage and transmitting the digitally recorded data to the memory upon a reproduction operation (Fig. 12, from 1394 to 310 to 250, with reference to Fig. 1 b).

Regarding claims 4-5, the combination with Chauvel further meets the limitations of:

- a transport stream processor (Fig. 1 B, "210, transport packet parser"), connected to the bus with an input for receiving coded audio-visual data from the input port (transport data input port);
- a host processor (Fig. 2, "comm. Processor 280" and "ARM" col. 18, lines 58-, between both comm. and ARM they handle, user inputs such as IR/RF, wherein 280, in accord to col. 9, is communication co-processors", wherein the ARM handles interrupts), connected to the bus as shown in Fig. 1 b and the memory for performing graphical user interface and browser functions (deemed met by, handling

Art Unit: 2616

user inputs for various functions, associated with services and recording and reproduction operations, etc.....);

- user inputs for various functions, associated with services and recording and reproduction operations, etc.....);
- an interface (bus interface between element recited etc.), for receiving from the transport (Fig. 1 B, "210") and for transferring and received data simultaneously to the memory (of the traffic controller or memory 240, see col. 17 and claim 1), via the bus and to the decoder (from traffic controllers memory), wherein the memory includes buffer space for temp storage from the interface;
- wherein the host processor or ARM in combination with the traffic controller, directing the memory to transfer coded data to be recorded to the recording device; and
- the interface receives the coded data from the recording device via the memory and bus (Fig. 1 b and Fig. 12);
- wherein the interface is adapted to transfer coded data to the decoder, claim 5.

Regarding claim 6, the combination as applied provides for MPEG GOP video data structure (col. 6 of Muto GOP), such that the decoder receives successive GOPs during a reproduction operation (Forward Play), wherein it is deemed obvious a graphics accelerator can be provided with a memory and operate substantially the same as Muto, wherein the accelerator allow for offloading processing from the main processing element, further it is deemed met that while decoding outputting images of a GOP, that the decoding would be processing the NEXT/Previous depending upon the mode, while outputting an associated related in time at least one frame of a successive or prior GOP, as shown in Fig. 1 of Muto, the decoding element has a code buffer and frame buffer with areas 1-4, therefore, it is deemed that a successive or previous would be loaded to the code buffer 2-1 and decoding, while outputting at least one frame from frame buffer memories {2-3 1-4} further based on the knowledge of MPEG having various time stamps, such as:

- DTS (decoding time stamp), which dictates the time to enter the decoder associated with,

Art Unit: 2616

- a PTS which indicates the time to present the data from the decoding element for presentation, also reference Fig. 5, which shows the storage relationship between the frame and code buffers, reference row code buffer 1I, wherein frame buffer has decoded 16 I of next GOP in view of Fig. 2, I GD or gop = 15 frames, also reference 4 A, as understood by the examiner.

Regarding claims 7-8, the combination with Muto provides for playback using I and/or I & P, I, P & B (col. 3, also reference Fig. 3 e, "28 P, 27 B ..... 16 I", all three picture types).

Claims 9-11, 18-23, 28, 32-33 are analyzed and discussed with respect to the claims above.

Regarding claim 12, the combination with Muto further meets the limitation of a present delay is inserted at the beginning of the displayed reverse playback (Muto, Fig. 4 A, "after lapse of IV from Vsync used to start decoding picture 28 p.").

Regarding claim 15, the combination with Muto, further meets the limitations of an engine with a buffer and memory interface (Muto fig. 1, "code buffer and frame buffer") and an encoder for processing decoded to the display on 3 in forward or reverse modes of operation.

Regarding claim 37 based on the combination as applied, fails to disclose wherein the second memory size of at least X, wherein  $X = (NI + Mp) * bufsize(Mbytes)$ , wherein  $(NI + Mp)$  = number of I frames and P frames in a GOP and bufsize equal to the product of the image size times the bit depth of the decoded images.

The examiner takes official notice that selecting a buffer size is based on the decoded image sizes and the number of frames desired to be worked with at one time in the decoded frame memories, as shown Muto provides different embodiment with different number of buffer elements, Fig. 5, 4 frame buffer elements, Fig. 6, 3 buffer elements, Fig. 14 5 frame buffer elements, wherein each element must hold either an I or a P, therefore, it would have been obvious based on the number of memory elements holding decoded frames, to provide buffer size based on the expected size of I pictures to dictate the at least the size required to perform the job as is obvious to those skilled in the art with Muto in front of them, wherein it is

Art Unit: 2616

further obvious to utilize the largest calculated or sensed image size, thereafter multiple by the number of desired decoded frames one skilled in the art would like to work with (reference Muto), as is obvious, to dictate buffer minimum space, being a safe minimum.

Regarding claim 38-39, the combination fails to disclose details of buffer size, such as recited about .5 M byte and further the mass storage being one of Hard Disk, magnetic storage {also reads on a hard disk} or optical.

The examiner takes official notice that a selecting a buffer size such as about .5 M byte is an obvious design choice to those skilled in the art, further other mass storage devices are also obvious to one skilled in the art, therefore, it would have been obvious to utilize a buffer about .5 M byte and to further utilize well known storage such as a hard disc being obvious design choices to those skilled in the art, being well known selections, for storage and buffer capacity issues based on the coded data itself, such as format, number of lines, data rate and type of coding used, as is obvious to those skilled in the art.

**Allowable Subject Matter**

1. Claims 13-14, 16-17, 24-25, 26-27, 29-30, 31, 34-36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

2. The following is a statement of reasons for the indication of allowable subject matter:

Regarding claims 13-14, 24-25, 29-30, 34-35, the prior art fails to disclose teach, or suggest, calculating a delay of t seconds is inserted at the beginning of the displayed reverse playback and wherein

- $t = (Nl + Mp) * FT(sec)$ ,  $(Nl + Mp)$  being equal to the number of I and P frames in a GOP, and  $Ft$  being the frame time, claims 13, 24, 29, 34;
- $t = (Nl + Mp + IB) * FT(sec)$ ,  $(Nl + Mp + IB)$ , being equal to the number of I, P and B frames in a GOP, and  $Ft$  being the frame time, claims 14, 25, 30, 35.

Regarding claims 16, 26, 31 and 36, the prior art fails to teach, disclose or fairly suggest in combination with their independent claims, when playback is accomplished (16 & 1) & (18 & 26), in the reverse direction up to N times {playback speed}, wherein N equals the number

of B frames intervening between I & P and/or successive P frames in the GOP + 1.

**Contact Fax Information**

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks  
Washington, D.C. 20231

or faxed to:

(703) 872-9314, (for formal communication intended for entry)

or:

(703) 308-5359, (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA., Sixth Floor (Receptionist).

**Contact Information**

3. Any inquiry concerning this communication or earlier communications should be directed to the examiner of record, Monday-Thursday, 8:00 AM to 5:00 PM Vincent F. Boccio (703) 306-3022.

Any inquiry of a general nature or relating to the status of this application should be directed to Customer Service (703) 306-0377.

Primary Examiner, Boccio, Vincent  
12/11/04

  
VINCENT BOCCIO  
PRIMARY EXAMINER